Timetable for Minor in Electronics Engineering (VLSI Design) (JULY– DEC 2026)

Day	1 (8:00-8:50)	2 (8:50 - 9:40)	3 (9:40-10:30)	4 (10:30-11:20)	5 (11:20-12:10)	6 (12:10-1:00)	7 (1:00-1:50)	8 (1:50-2:40)	9 (2:40-3:30)	10 (3:30-4:20)	11 (4:20-5:10)	12 (5:10-6:00)	13 (6:00-6:50)
Monday												EDIC (L) AKC F209	EDIC (L) AKC F209
Tuesday												DSD (P) (FPGA Lab C325, C Block)	
Wednesday												DSD (L) RPN F209	DSD (L) RPN F209
Thursday												DSD (L) RPN F209	EDIC (L) AKC F209
Friday												EDIC (P) (EL Lab, C212, C Block)	

Sr. No	Course	Faculty	Mobile	Email
1	Electronic Devices for Integrated Circuits (EDIC)	Dr. Arun Kumar Chatterjee (AKC)	9501493957	arun.chatterjee@thapar.edu
2	Digital System Design (DSD)	Dr. Rishikesh Pandey (RPN)	7973414740	rpandey@thapar.edu

Sr. No	Course	Lab Technicians	Mobile	Email
1	Electronic Devices for Integrated Circuits (EDIC)	Mr. Rampal	6280501150	rampal.yadav@thapar.edu
2	Digital System Design (DSD)	Mr. Rahul	7837643404	rahul.kumar@thapar.edu

Sr. No	Course	Lab Attendant	Mobile
1	Electronic Devices for Integrated Circuits (EDIC)	Mr. Vijay	9464655095
2	Digital System Design (DSD)	Mr. Vijay	9464655095